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| 09/534,812 | 03/24/2000 | Shunpei Yamazaki | SEL 169 | 2789 |

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COOK ALEX McFARRON MANZO CUMMINGS & MEHLER LTD.
200 West Adams Street Suite 2850
Chicago, IL 60606

| EXAMINER | |
|---|---|
| NGUYEN, KEVIN M | |

| ART UNIT | PAPER NUMBER |
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| 2674 | 21 |

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/534,812 | Applicant(s) YAMAZAKI | |
|---|---|---|---|
| | Examiner Kevin M. Nguyen | Art Unit 2674 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,51,53 and 55-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,51,53 and 55-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. The amendment filed on 03/01/2004 is entered. The rejection of claims 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 51, 53, and 55-68 are maintained. New claims 69-74 are necessitated the new ground of rejection.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 5 and 55-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al (US 6,020869) in view of Nakai et al (US 6,072,454).

3. As to claims 1 and 55-57, Sasaki et al teach an active matrix liquid crystal display device TFT-LCD (11) associating a method thereof, the device comprising an X-driver 101, Y-driver 201, an opposing substrate and electrode, a gray-level control circuit (331) controls 5-bit input to a 3-bit output, and 2-bit data is used to select by the selection circuit (341) the time ratio gray scale 1/4, 2/4, 3/4, 4/4, and 5/4 (311, 313, 315, 317, 319), then processing 3-bit data and 2-bit data at the same time that are controlled by the processing circuit (351) (see figure 39, col. 36, lines 23-34, col. 37, lines 40-55, and col. 52, lines 10-11), as satisfying the condition (m-n)= (5-3) bit as information for time ratio gray scale, and m>n (5>3).

Sasaki et al fail to teach optically compensated mode (OCB mode). However, Nakai et al teach an OCB mode liquid crystal may also use arbitrary, and any type to

LCD (col. 16, line 65 through col. 17, line 9). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize an OCB mode liquid crystal taught by Nakai et al for Sasaki et al's LCD because this would improve the quality of the image being displayed, while saving power consumption (col. 13, lines 1-6 of Nakai et al).

4. As to claims 3, 5 and 58, Sasaki et al teach a TFT-LCD device (11) associating a method thereof, the device comprising an X-driver 101, Y-driver 201, an opposing substrate and electrode, a gray-level control circuit (331) controls 5-bit input to a 3-bit output, and 2-bit data is used to select by the selection circuit (341) the time ratio gray scale ¼, 2/4, ¾, 4/4, and 5/4 (311, 313, 315, 317, 319), then processing 3-bit data and 2-bit data at the same time that are controlled by the processing circuit (351) (see figure 39, col. 36, lines 23-34, col. 37, lines 40-55, and col. 52, lines 10-11), as satisfying the condition (m-n)= (5-3) bit as information for time ratio gray scale, and m>n (5>3);

forming an image for one frame (F) image comprising $2^{m-n}$ subframes "four-frame period control (A)" by performing voltage grayscale method and time ratio grayscale that use (m-n) bit at the same time, and

applying voltage which makes an orientation of liquid crystal to a bend orientation on starting display of the $2^{m-n}$ subframe "four-frame period control (A)" (see figures 42 and 43, column 37, lines 30-39).

As to claims 59-64, Sasaki et al teach a TFT-LCD panel (11) which includes a liquid crystal cell $C_{LC}$ (41) on the substrate coupling to an opposing (or counter, common) electrode driving circuit (see figure 39).

5. Claims 19, 21, 23, 25, 27, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al in view of Nakai et al, and further in view of McKechnie et al (US 4,864,390).

As to claims 19, 21, 23, 25, 27 and 29, Sasaki et al and Nakai et al teach all of the claimed limitation of claims 1, 3 and 5, except for "a rear projector and a front projector comprise three liquid crystal display devices. However, McKechnie et al teach three LCDs onto the rear projector and the front projector (see column 5, lines 24-27). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the LCD of Sasaki et al's and Nakai et al's in the rear projector and the front projector of McKechnie et al's because this would be applied to various types of the rear projector and the front projector (col. 3, lines 13-15 of McKechnie et al).

6. Claims 7, 9, 11, 13, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al in view of Nakai et al as applied to claims 1, 3, and 5 above, and further in view of Ishida et al (US 6,069,609).

As to claims 7, 9, 11, 13, 15 and 17, Sasaki et al and Nakai et al teach all of the claimed limitation of claims 1, 3, and 5, except for the positive number m is 10 and 12 and the positive number n is 2 and 4. However, Ishida et al teach a gray scale circuit having a n bit input data signal and m bit output data signal (figure 26) with $m<n$ (col. 2, line 44). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the n bit input and m bit output taught by Ishida et al for the gray scale circuit 301 of Sasaki in order to assign m is 10 and 12 and n is 2 and 4.

7. Claims 49, 51, 53 and 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al in view of Nakai et al as applied to claim 1 above, and further in view of Kusano et al (US 5,677,704).

As to claims 49, 51, 53 and 65-68, Sasaki et al and Nakai et al teach all of the claimed limitations of claims 1, 3 and 5, except for a notebook type personal computer/ a mobile computer. However, Kusano et al teach a liquid crystal display device being applied to the laptop computer 10 (figure 1, col. 5, lines 16-18). It would have been obvious to a person of ordinary skill in the art at the time of the invention to utilize the laptop computer 10 taught by Kusano et al for the LCD of Sasaki et al because a laptop computer 10 including LCD 16 is applicable to the invention.

8. Claims 70-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al (previously cited) in view of Nakai et al (previously cited), and further in view of Yamaguchi et al (newly cited, US 6,222,515),

As to claims 70-74, Sasaki and Nakai teaches all of the claimed limitations, except for a display gray scale level is obtained by totaling gray scale voltage levels in sub-frame terms of one frame and then averaging totaled gray scale voltage levels by said time ratio gray scale.

However, Yamaguchi teaches a liquid crystal display device comprising gray-scale levels 1-4 are realized by applying 2 (V), 2 (V), 6 (V), 6 (V) to the first field and 2 (V), 4 (V), 2 (V) 4 (V) to the second field to produce a mean effective voltage of 2 (V), 3 (V), 4 (V), 5 (V), respectively, for the one frame (figs. 7A-7D, col. 8, lines 15-27).

Hatching in FIGS. 7A to 7D shows this mean effective voltage (a display gray scale level).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Sasaki's sub-field including the gray-scale levels 1-4 are realized by applying 2 (V), 2 (V), 6 (V), 6 (V) to the first field and 2 (V), 4 (V), 2 (V) 4 (V) to the second field to produce a mean effective voltage of 2 (V), 3 (V), 4 (V), 5 (V), respectively, for the one frame, in view of the teaching in the Yamaguchi's reference because this would improve the quality of the image being displayed without increasing a circuit scale as taught by Yamaguchi (col. 2, lines 41-45).

***Response to Arguments***

9. Applicant's arguments filed 03/01/2004 have been fully considered but they are not persuasive.

10. In response to applicant's argument that claim 1 recite "conducting voltage gray scale and time ration gray scale at the same time by using n bit out of m bit digital data as information for voltage gray scale, and (m-n) bit as information for time ratio gray scale." This argument is not persuasive because Sasaki teaches the selection circuit 341 is designed to select one of the first to fifth gray-level pattern generating circuit 311, 313, 315, 317 and 319 in accordance with an output from the gray-level control circuit 331 when the externally input 5-bit gray-level display data corresponds to the intermediate gray level between the gray-level voltages preset in the gray-level voltage generating circuit 501 (fig. 39, col. 37, lines 23-30).

Therefore, the 1/4 gray level, the 2/4 gray level, and the 3/4 gray level correspond to the time ratio gray scale as claimed, and the gray-level voltage generating circuit 501 corresponds to voltage gray scale as claimed.

11. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., totaling the gray scale voltage levels in the sub-frame line terms and then time-averaging the total in one frame) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

12. In response to applicant's argument that claims 3, 5 and 58 recite "applying a voltage which makes an orientation of liquid crystal to a bend orientation on starting display of the $2^{m-n}$ subframes".

This argument is not persuasive because Sasaki teaches recited in 3rd paragraph above, processing 3-bit data and 2-bit data at the same time that are controlled by the processing circuit (351) (see figure 39, col. 36, lines 23-34, col. 37, lines 40-55, and col. 52, lines 10-11), as satisfying the condition (m-n)= (5-3) bit as information for time ratio gray scale, and m>n (5>3). Recited in col. 38, lines 39-40, since the control of the frame (F) periods is effects in combination with the eight gray-level voltages. Therefore, forming one frame $F= 2^{5-2}= 8$ subframes as claimed.

Nakai teaches the host liquid crystal turned by 90 to 360 degrees which is oriented at random are effective in enhancing contrast and reflectance. An OCB mode

liquid crystal may be used (col. 16, lines 59-62). Vth1<Vth2<Vth3 and a voltage indicated by reference numeral 816 exceeds Vth1, the signal of the signal lines 809 is applied to the liquid crystal layer 812 (col. 18, line 66 to col. 19, line 1).

Therefore, the combined teaching of Sasaki and Nakai meet the claimed limitations above.

For these reasons, the rejections based on Sasaki et al and Nakai et al have been maintained.

***Conclusion***

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
May 21, 2004

XIAO WU
PRIMARY EXAMINER